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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO
09/819,990	03/29/2001	Isao Minematsu	57454-060	3710
7590 08/22/2005			EXAMINER	
McDERMOTT, WILL & EMERY			PAN, DANIEL H	
600 13th Street, N. W. Washington, DC 20005-3096			ART UNIT	PAPER NUMBER
			2183	•
		DATE MAILED: 08/22/2005		

Please find below and/or attached an Office communication concerning this application or proceeding.

1						
	Application No.	Applicant(s)				
Office Astion Comments	09/819,990	MINEMATSU, ISAO				
Office Action Summary	Examiner	Art Unit				
	Daniel Pan	2183				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence address				
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply if NO period for reply is specified above, the maximum statutory period versions after the reply within the set or extended period for reply will, by statute, any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be tim y within the statutory minimum of thirty (30) days vill apply and will expire SIX (6) MONTHS from , cause the application to become ABANDONE	nely filed s will be considered timely. the mailing date of this communication. D (35 U.S.C. § 133).				
Status						
2a) ☐ This action is <b>FINAL</b> . 2b) ☐ This 3) ☐ Since this application is in condition for alloware	<i>,</i> —					
	.x parte Quayle, 1955 C.D. 11, 40	30 O.G. 210.				
Disposition of Claims  AND Claim(a) 1.40 in/ore pending in the application						
<ul> <li>4) Claim(s) 1-10 is/are pending in the application.</li> <li>4a) Of the above claim(s) 11-14 is/are withdrawn from consideration.</li> <li>5) Claim(s) is/are allowed.</li> <li>6) Claim(s) 1-10 is/are rejected.</li> <li>7) Claim(s) is/are objected to.</li> <li>Claim(s) are subject to restriction and/or election requirement.</li> </ul>						
Application Papers						
9)☐ The specification is objected to by the Examine 10)☑ The drawing(s) filed on 29 March 2001 is/are:  Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct 11)☐ The oath or declaration is objected to by the Examine 11.	a)⊠ accepted or b)□ objected to drawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).				
Priority under 35 U.S.C. § 119						
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:  1. Certified copies of the priority document: 2. Certified copies of the priority document: 3. Copies of the certified copies of the priority document: application from the International Bureau * See the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	on No ed in this National Stage				
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:					

U.S. Patent and Trademark Office PTOL-326 (Rev. 1-04)

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1. Upon further review and consideration into the remarks made by applicant in the Brief, the finality of the last Office action on 12/21/04 has been withdrawn. Claims 1-10

remain for examination. Claims 11-14 have been canceled on 03/21/05. This is a non-

final action.

2. In view of the Appeal Brief filed on 06/15/05, PROSECUTION IS HEREBY

REOPENED. A new ground of rejection is set forth below.

3. To avoid abandonment of the application, appellant must exercise one of the

following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply

under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied

by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130,

1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United

States.

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- 4. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Boggs et al. (5,687,338).
- 5. As to claim 1, the language of "single said instruction code" is read as a macroinstruction, or the like, in view of the applicant's specification in page 3, lines 22-29. Boggs taught:
- a) a program control unit controlling fetch of an instruction code (see the instruction fetch unit 102 in fig.1);
- b) an instruction decode unit decoding said fetched instruction code (see the decode unit 106 in fig.1, see col.16, lines 63-67, col.17, lines 1-11, lines 18-25);
- c) an address operation unit [112] [114] operating an address (see the mapping of the address in col.10, lines 9-34) of a memory on the basis of the result of decoding by said instruction decode unit; and
- d) a data operation unit operating data on the basis of the result of decoding by the instruction decode unit (see decoding of FAR\_CALL in col.18, lines 31-67, see also ADD instruction for another example), wherein the data operation unit executed data transfer between registers (see UIP 2) and data transfer between said register and said memory (see reading at the address pointed by CR0 to t register in UIP 1) in correspondence to single the instruction code (macro code, see also the examples of single microinstruction, ADD or FAR\_CALL in col.6, lines 20-67). having a single operation code fetched by said program control unit.
- 6. See also ADD single opcode included data transfer between memory (mem) and register (t), and transfer between the register (t) and a register (eax).

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The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 7. Claims 2-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Boggs et al. (5,687,338) in view of Kudo (6,560,692).
- 8. As to claim 2, 7. limitatins of claim 1 have been already discussed in paragraph 5 above. Boggs did not specifically show the data transfer from the first register to the memory and the transfer from a second register to the first register as claimed. However, Kudo also disclosed transfer of the data from a first register (general purpose) to a memory (stack) and transfer the data from a second register (special register) to the first register (general purpose register) (e.g. see transfer of data by push col.26, lines 30-35). It would have been obvious to one of ordinary skill in the art to use Kudo in Boggs for the data transfer from the first register to the memory and the transfer from a second register to the first register as claimed because the use of Kudo could increase the ability of Boggs to accept the data in a predefined sequence between the registers and memory, thereby increasing adaptability of a given system data flow command (such as push) to specific a data resource (register and memory), and therefore, provided motivation.
- 9. As to claims 3, 7, Kudo also decremented and incremented the pointer (e.g. see the update of the SP in col.13, lines 9-43).

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10. As to claims 4.8, first register of Kudo was a working register (general purpose).

- 11. As to claims 5,9, Kudo's second register was a control register (special register).
- 12. As to claim 6, Boggs did not specifically show the pop instruction as claimed. However, Kudo also taught transfer of the data in first register to second and the transfer in memory to the first (see the transfer of data by pop instruction in col.26,lines 30-35). It would have been obvious to one of ordinary skill in the are to use pop instruction as claimed because the use of Kido in Boggs could expand the options of the instruction codes based on the predetermined requirement of the system, and because Boggs also taught the prediction of branch instructions (see col.13, lines 49-67), which was a suggestion of the need for including a pop instruction, or the like, in order to return the processing condition on the predicated path, and for the above reasons provided a motivation.
- 13. As to claim 10, Kudo also kept the value of stack pointer unchanged for a single push (e.g. see the latched stack pointer value in latch (Add LT) 32 at the end of the push col.27, lines 10-30).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

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14. Claim 1 rejected under 35 U.S.C. 103(a) as being unpatentable over Morrison et al. (5,918,031) in view of Geldman et al. (5,524,268).

As to claim 1, as to the "single said instruction code" in the claim, it is read as a 15. macroinstruction in view of applicant's specification page 3, lines 22-29. See also applicant's drawing in fig.9 and fig.10, the push was actually two push instruction codes: push R0 and push AR0. The opcodes (push) were the same, but the instruction codes (push R0 and push AR0) were not the same, therefore, there were two instruction codes, not a single instruction code. Morrison taught a system in which a common sequence of instructions were collapsed into a single code (see col.5, lines 22-37, col.8, lines 30-35) including at least a data transfer system for transferring between the register and memory (see MOV reg, mem in col.7, line 35). Morrison did not explicitly show the data transfer between the registers as claimed. However, Geldman disclosed a single code (single instruction) for transfer between registers (see col.8, lines 16-19). It would have been obvious to one of ordinary skill in the art to use Geldman in Morrison for including the operation of transfer between the registers as claimed because the use of Geldman could provide Morrison the ability to operate more than one operation transfer into a single instruction format, therefore, reducing the hardware space of the system, and because Morison did indicate the use for collapsing instructions into a single instruction code (see col.8, lines 30-35) in order to minimize the hardware space, and for the above reasons provided a motivation.

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Morrison is used as primary reference because it showed clearly the data transfer between memory and register. Geldman is used to show the clear teaching of data transfer between registers which was not explicitly taught by Morrison.

16. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kudo (6,560,692) in view of The MCS-80/85 Family User's Manual, page 5-2, 5-3, 5-15, Intel, 1986.

## 17. As to claim 1, Kudo disclosed at least:

- a) program control unit for fetching instructions (fetching of the instruction no explicitly shown)
- b) instruction decoder for decoding the instructions (col.11, lines 40-61 for the decoding of the specific stack pointer instructions, see also col.23, lines 22-23, col.26, lines 60-64);
- c) address operation unit on the basis of the decoding result (col.26, lines 36-56 for the address selection;
- d) data operating unit executed the transfer between registers and a memory Stack) in response to a single instruction code (see the data transfer between the register and the stack memory by the push instruction in col.15, lines 20-28, col.25, lines 29-67, see also the transfer of the special register to general purpose register in col.26, lines 30-35, see also all other specific stack pointer instructions in col.14, lines 44-53).

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- 18. Kudo did not specifically teach the transfer between the registers and between the register and the memory on the single instruction code as claimed. However, the MCS-80/85 Family User's Manual, Intel., 1986 ("Intel" hereafter) taught transfer between register [rh] and memory (SP-1) and transfer between registers (SP register and r register) corresponding to a single instruction code [PUS rp.] (see page 5-2, 5-3, 5-15, see immediate value stored in data register, r, in page 5-3). It would have been obvious to one of ordinary skill in the art to use Intel in Kudo for transferring the transfer between the registers and between the register and the memory on the single instruction code as claimed because the use of Intel could provide Kudo the ability to accept data value in a predefined instruction format, thereby eliminating extra circuit space for the instructions and because Kudo did taught the use of a push instruction (col.15, lines 20-28), which was an indicating of the need for include the transfer between the registers such as one taught by Intel for minimize the hardware overheads (see page 5-15, (SP) <- SP-2), and in doing so provided a motivation.
- 19. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- a) Col et al. (6,209,082) is cited for showing the teaching of a single instruction code for plurality of data transfer operations (see col.10, lines 41-67, col.11, lines 1-8, see also following cycles of transfer in col.11, 12).

Kudo (6,560,692) and Geldman et al. (5,524,268) were prior art on the record, therefore, copies are not being provided herein.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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